

PATENT NUMBER

## U.S. UTILITY Patent Application

OIP/PE

PATENT DATE



APPLICATION NO. 09/943184	CONT/PRIOR	CLASS 365-251	SUBCLASS 315	ART UNIT 2818	EXAMINER TU HO
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APPLICANTS  
Leonard Forbes  
Jerome Eldridge  
Kie Ahn

TITLE  
Programmable array logic or memory devices with asymmetrical tunnel barriers

PTO-2040  
12/99

## ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	314	257	315	239			
INTERNATIONAL CLASSIFICATION							
H01L	29/76						

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL  
DISCLAIMER

☐ The term of this patent  
subsequent to \_\_\_\_\_ (date)  
has been disclaimed.

☐ The term of this patent shall  
not extend beyond the expiration date  
of U.S. Patent No. \_\_\_\_\_

☐ The terminal \_\_\_\_\_ months of  
this patent have been disclaimed.

## DRAWINGS

Sheets Drwg. 18	Figs. Drwg. 27	Print Fig. 2
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## CLAIMS ALLOWED

Total Claims 23	Print Claim for O.G. 1
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## NOTICE OF ALLOWANCE MAILED

2-13-04

## ISSUE FEE

Amount Due \$1630	Date Paid
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## ISSUE BATCH NUMBER

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